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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/440,928	11/16/1999	NOBUTOSHI AOKI	040301/0578	3624

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RICHARD L SCHWAAB
FOLEY & LARDNER
WASHINGTON HARBOUR
3000 K STREET NW SUITE 500
WASHINGTON, DC 200075109

EXAMINER	
RAO, SHRINIVAS H	
ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 02/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/440,928	AOKI ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,15-21,23 and 25-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-11,15-21,23 and 25-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 November 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

Receipt is acknowledged of paper submitted under 35 U.S.C. 120 claiming priority from U.S. Serial No. 09/440,928 filed on November 16, 1999 which itself claims priority from Japanese Patent Application No. P-10 –326973 filed On November 17, 1998, which papers have been placed of record in the file.

Continued Prosecution Application

The request filed on 11/19/2002 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 09/440,928 is acceptable and a CPA has been established. An action on the CPA follows.

Preliminary Amendment Status

Acknowledgment is made of entry of preliminary amendment filed 11/19 / 2002 that has been entered on December 19, 2002.

Therefore claims 1,4,11,15, 23 as amended by the amendment, claims 2-10,16-21, 25-31 as originally filed and claims 32 and 33 presently newly added are currently pending in the application.

Specification

The drawing corrections required in the PTO-948 (draftsman's review) enclosed with the Office Action of November 26, 2001 have not yet be overcome.

Applicants' are reminded of the changes to drawing requirements that mandate a drawing correction with the next response and that drawings corrections cannot be held in abeyance. Failure to correct drawings may result in the abandonment of the application.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 33 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The phrase "an element isolation region formed surrounding the insulated gate filed effect transistor, and having an insulating film embedded in a trench." Was not described in the specification as originally filed because the term "an element isolation region " is shown for e.g. in figure 1 # 2 and described in the specification page 16 lines 18 to 25 shows it to be a STI which does not surround the insulated gate filed effect transistor.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-11, 15-21, 23 and 25-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burghartz (U.S. Patent No. 5,583,059, herein after Burghartz) previously applied and Herbots et al. (U.S. Patent No. 5,241,214, herein after Herbots).

With respect to claim 1, Burghartz describes a semiconductor device including: a pair of main electrodes used as source and drain electrode (Burghartz fig. 1, 8 col. 3 lines 55-56, etc.).

Burghartz does not specifically mention/describe a channel forming region provided between a pair of main electrodes (but it is inherent that all FEts devices have a channel between the source and drain electrodes).

However, Herbots in figure 1 C, etc. and col. 5 lines 31 to 36 describes a channel region between the source and drain to complete the formation of the FET.
Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Herbot's channel in Burghatz's device to complete the formation of a FET.

The remaining elements of claim 1 are:

An insulating gate film formed on the channel forming region (Herbots Fig. 1C 16, 18), a gate electrode formed on the insulating gate film (Herbots Fig. 1 C 3 20) and provided with a first region of at least a first group IV element (Burghatz Fig. 2 A #7 col.

3 line 37, Herbots fig. 2 # 115) and a second group IV element and formed in contact with the insulating gate film (Burghartz fig. 2 A # 4-5 col. 4 line 67) and a second region including the first group Iv element and formed on the first region, the first and second regions having an identical conductivity type. (Burghartz fig. 2 a # 6, col. 4 line 50).

With respect to claims 2 and 3, Burghartz describes a semiconductor integrated circuit including: wherein the first region has a composition ratio of the second group IV element gradually reduced with a distance from the insulated film (Burghartz col. 5 lines 4-8). (Cl. 2); step wise reduction (Fig. 3 C-E).

With respect to claim 4, Burghartz describes a semiconductor integrated circuit including : claim 4 recites the elements of claim 1 and further recites a silicide electrode formed in contact with the second region of the gate electrode Fig. 3 E # 8 A, 7A, 10 A, col. 6 line 10-12) and being substantially free from the second group IV element (col. 5 line 49-56).

With respect to claim 5, Burghartz describes a semiconductor integrated circuit including : the first and second group IV elements being silicon and germanium. (col. 4 line 56 and col. 5 line 16-17)or group IV alloys . (Herbots in its abstract describes MOSFETs wherein the device (gates) are formed of Group IV alloys (i.e. alloys of Titanium etc in col. 2 line 40-43).

With respect to claim 6, Burghartz and Herbots describe a semiconductor integrated circuit including : a gate electrode having a thickness larger than a width of the depletion layer of the Si gate electrode (Burghatz col. 5 lines 1-10).

With respect to claim 7, Burghartz and Herbots describe a semiconductor integrated circuit including :wherein the composition ratio of Ge in the first region is at least 0.1 or larger. (Burghatz col. 4 line 67 and col. 5 line 6).

With respect to claims 8 and 9 , Burghartz and Herbots describe a semiconductor integrated circuit including : wherein Boron and Arsenic are used . (Burghartz col. 5 line 23- Arsenic, col. 5 line 67- Boron).

With respect to claim 10, Burghartz and Herbots describe a semiconductor integrated circuit including : wherein the group Iv element used is carbon instead of Germanium. See claim 5 above Herbots teaches the use of all group he elements (alloys) interchangeably and as C is a group Iv compound, Herbots describes its use instead of germanium.

With respect to claim 11, Burghartz and Herbots describe a semiconductor integrated circuit including : wherein the elements of claims 1 and 4 are recited and further the second region is specified to be composed of multiple element compound consisting of first and second group elements and metal (i.e. alloys of group IV compounds- see Herbots description stated under claim 5 above).

With respect to claims 15 and 16, Burghartz and Herbots describe a semiconductor integrated circuit including : claim recites the elements of claims 1 and 4 and specifies the first and second group Iv region to be an epitaxial layer Col. 4 line 55).(cl. 15) and an elevated source and drain (Burghatz fig. 1).

Claims 17-21 repeat the elements of claims 7-10, and are rejected at least fur the reasons stated above.

With respect to claim 23, Burghartz and Herbots describe a semiconductor integrated circuit including : claim 23 repeats the elements of claims 15 and further recites an elevated electrode having a third region formed of regions similar to the first and second regions (See Herbots fig. 3 b).

With respect to claims 25-27, Burghartz and Herbots describe a semiconductor integrated circuit including : forming a thin layer is added between insulated film and the first region and composed of the first or second group Iv element (Herbots fig. 1 A # 16 between first region 14 and insulated gate film 18).

With respect to claim 28 it repeats the elements of claims 15 and 23 and is rejected for reasons stated above under claims 15 and 23.

With 29-31, wherein the thickness of the layer is I nm or less (Herbots col. 4 lines 61-63).

With respect to claim 32, it repeats the elements of claim 23 and further adds that a second conductivity type insulated gate filed effect transistor having a pair of second conductivity type main electrodes used as source and drain electrodes, (Burghartz fig. 1 , pFET), a first conductivity type channel forming region provided between the pair of second conductivity type main electrodes (Herbots in figure !C , etc. and col. 5 lines 31 to 36) , a second insulating film formed on the first conductivity type channel forming region (Herbots fig. 1d, Burghartz fig. 1),and a second gate electrode formed on the second insulating gate film (Herbots fig. 1d , Burghartz fig. 1) and provided with w third region including at least the first group IV element and the second group IV element and formed in contact with the second insulating gate film and a fourth region including the

first group Iv element and formed on the third region, the third and fourth regions having an identical conductivity type. (same as claim 23 above).

B. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Burghartz (U.S. Patent No. 5,583,059, herein after Burghartz) previously applied and Herbots et al. (U.S. Patent No. 5,241,214, herein after Herbots) as applied to claims 1-11, 15-21, 23 and 25-32 above and further in view of Wang et al. (U.S. Patent No. .5,357,119 herein after Wang).previously cited but only now applied.

With respect to claim 33, it repeats the elements of claim 32 above and the above rejection is incorporate here by reference.

Burghartz and Herbots do not specifically mention the additional an element isolation region formed surrounding the insulated gate filed effect transistor (assuming arguendo that support can be found in the original specification) and having an insulating film embedded in a trench.

However, Wang in figures 1a to 2a etc. and col.2 lines 29-31describes a device isolation (element isolation region) formed surrounding the insulated gate field effect transistor and having an insulated film embedded therein to form devices using less space, without bird's beak problems and in CMOS devices prevent latch-up.

Therefore it would have been obvious to one of ordinary skill in the art to include Wang's a device isolation (element isolation region) formed surrounding the insulated gate filed effect transistor and having an insulated film embedded therein in Burghartz and Herbots' devices to form devices using less space, without bird's beak problems and in CMOS devices prevent latch-up.

Any inquiry concerning this communication should be directed to Steven H. Rao at telephone number 703-306-5945.

The fax/ phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Steven H. Rao

Patent Examiner
resubmitted
February 13, 2003.

LONG PHAM
PRIMARY EXAMINER